REMARKS

Preliminarily, Applicant thanks the Examiner for conducting the August 17, 2004 telephonic interview. The substance of this interview is reflects in the remarks below.

Claims 1-22 were examined, and all claims are rejected. Claims 1-12, 14, 15, 17, 18, 20, and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dao et al. (U.S. Patent No. 6,275,891) in view of Lowe et al. (U.S. Patent No. 6,173,243), and claims 13, 16, 19, and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dao et al. in view of Lowe et al. , and further in view of Stilp (U.S. Patent No. 6,097,336). Applicant respectfully traverses these rejections for the reasons set forth below.

The present invention is directed to a signal processing apparatus having a channel pooling signal processor 76 and a digital signal processor (DSP) 72, wherein the channel pooling signal processor 76 performs more computationally intensive signal processing operations than the DSP 72. The channel pooling signal processor 76 has a reconfigurable multiprocessor 66, which has computation units 36 and an interconnect mechanism 32, a test interface 34 for testing the function of the computation units 36, and a microprocessor 74 for managing data flow into and out of the channel pooling signal processor 76. The interconnect mechanism 32 connects the computation units 36, the interface 34, and the microprocessor 74. Each of the computation units 36 has a data sequencer 46 for controlling program execution, a configurable logic unit 44, and a dedicated memory 42.

The applied references do not suggest the claimed channel pooling signal processor, which is a specialized processor that is reconfigurable and designed to perform intensive mathematical processing. As claimed, and as shown in Figs. 2-5, the channel pooling signal processor 76 includes a reconfigurable multiprocessor having computation units 36, a test interface 34, a microprocessor 74, and an interconnect mechanism 32. Each of the computation units 36 includes a data sequencer 46, a configurable logic unit 44, and a dedicated memory 42.

Dao discloses a processing architecture in which a dedicated, custom-designed hardware accelerator is coupled to a DSP 108 and a DSP memory 110 via a DSP bus 112. The DSP 108 performs less demanding computationally-intensive tasks of pre-processing and post-processing data, and allows the hardware accelerator to perform specific processing steps that the DSP 108 is too inefficient to perform. Col. 1, line 61, to col. 2, line 12.

Contrary to the Examiner's position in the Office Action, Dao's hardware accelerator is not equivalent to the claimed channel pooling processor, which includes a reconfigurable multiprocessor. Dao's hardware accelerator is a dedicated, custom-designed device that carries out specific algorithms. (See Dao, col. 1, lines 61-64.) The claimed channel pooling processor, on the other hand, is reconfigurable. More specifically, the claimed channel pooling processor has a reconfigurable multiprocessor, which has computation units that are flexibly configured at least in part via their configurable logic units. This flexible configuration is advantageous over conventional devices in that they may be used to achieve different functions, thereby allowing processing for multiple modes of operation. See the application, for example, on page 3, lines 19 et seq., and page 9, lines 2-13. Thus, the claims are patentable over the applied references for at least this reason.

With further regard to claim 9, there is no suggestion in the applied references of an antenna for receiving communication signals. Thus, claim 9 is patentable for at least this additional reason. Further, claim 9 is specifically directed to a base station transceiver. There is no suggestion in the applied references of a base station transceiver. The Examiner asserts that because the base station transreceiver is recited in the preamble, it is not given any patentable weight. Applicant disagrees. The preamble is given weight if it is necessary to breathe life and meaning into the claim. This is the case with claim 9. The body of claim 9 recites an antenna for receiving communication signals, and this element only makes sense in the context of being included in a base station receiver. Claim 9 is therefore further patentable for this additional reason.

The Examiner stated during the interview that because he has not addressed the antenna recited in claim 9, he will issue a new non-final Office Action, that is, assuming he does not allow the application based on this Response.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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